Value-added Learning Platform for Undergraduate Electrical and Electronics Engineering Education

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ABSTRACT

This paper shows how to shorten the learning curve for FPGA training once they enter the workforce. The demands for academic institutions to equip graduate engineers with VLSI and FPGA prototyping skills and knowledge are increasing Simply including the topic in digital subject courses is no longer sufficient. In this paper, the development of an FPGA-based three-month training program by KDU College Engineering Department to bridge this gap in skills will be described. Due to government-industry-academe collaboration, the ongoing program has produced encouraging results: 1) design, development and presentation of arcade-type console games; 2) the culture of independent learning among participants; 3) increase in depth and quality of undergraduate final year projects; and 4) improvement in participants' soft skills, time-management and teamwork.

Keywords: *VLSI, FPGA (field-programmable gate array), Industry-academe collaboration, training program.*

INTRODUCTION

Electrical and Electronics Engineering has always thrived in developing new concepts and designs. New, powerful and highly advanced devices emerge in the commercial market almost daily. The key component to this trend has been the powerful chip inside each device. Faster, smaller and more powerful microprocessors and microcontrollers are being created to satisfy the customers' needs for speed, better performance and smaller size requirements. The high demand for netbooks and mobile phones, LCDs, semiconductor equipment and integrated circuits (ICs) is putting pressure on manufacturers and multinational companies to increase output and production. This has allowed the electronics industry to get out of the slump caused by the recession as shown in Figure 1 cited in the article "Good beginning next year say chips and electronics firms" (Tan, 2009). All this translates to an increasing need for manufacturing workers and engineers.

Global Semiconductor Capital Equipment Spending Forecast
(US$bil)

	2009	2010	2011	2012	2013	2014
Semiconductor	25.3	36.7	47.8	56.9	48.7	53.6
Capital Equipment	16.3	25.5	32.7	38.6	31.5	35.6
Wafer Fab Equipment	12.6	19.7	25.5	30.5	25.3	28.5
Packaging and Assembly Equipment	2.4	3.6	4.6	5.3	4.0	4.7
Automated Test Equipment	1.3	2.2	2.6	2.8	2.2	2.4
Other Spending	8.9	11.3	15.2	18.4	17.3	18.0

Source: Gartner (Dec 2009)

Figure 1: Global spending forecast.

While the demand from the industry is present, the manpower requirement is not matched by what the academic community produces. According to Professor Lee, director of Universiti Tunku Abdul Rahman Institute of Postgraduate Studies and Research, "There aren't enough qualified research and design engineers to meet the demand of multinational companies (MNCs)"(Lim, 2009). Simply put, employees fresh from their studies do not have the skills and technical competency companies seek. In today's competitive job market, substantial hands-on experience and exposure to electronic design automation (EDA) tools are a must. For companies, prospective engineers with these credentials are highly desirable because it shortens training time when these graduates enter their organisation as newly-hired employees.

This dilemma is quite evident in chip designing and manufacturing, specifically in the area of Very Large Scale Integration (VLSI) designing and Field Programmable Gate Array (FPGA) prototyping. While most institutes of higher learning (IHLs) in Malaysia include these topics in digital design courses as part of their course material and content, it has not approached the level that the industry requires.

VLSI AND FPGA EDUCATION

Circuit density is tracked by the integration level, which is the number of components in a circuit. Integration levels (Table 1) range from small scale integration (SSI) to very large scale integration (VLSI). Very Large Scale Integration (VLSI) refers to placing one hundred thousand or more transistors in a single chip (Palnitkar, 2003).

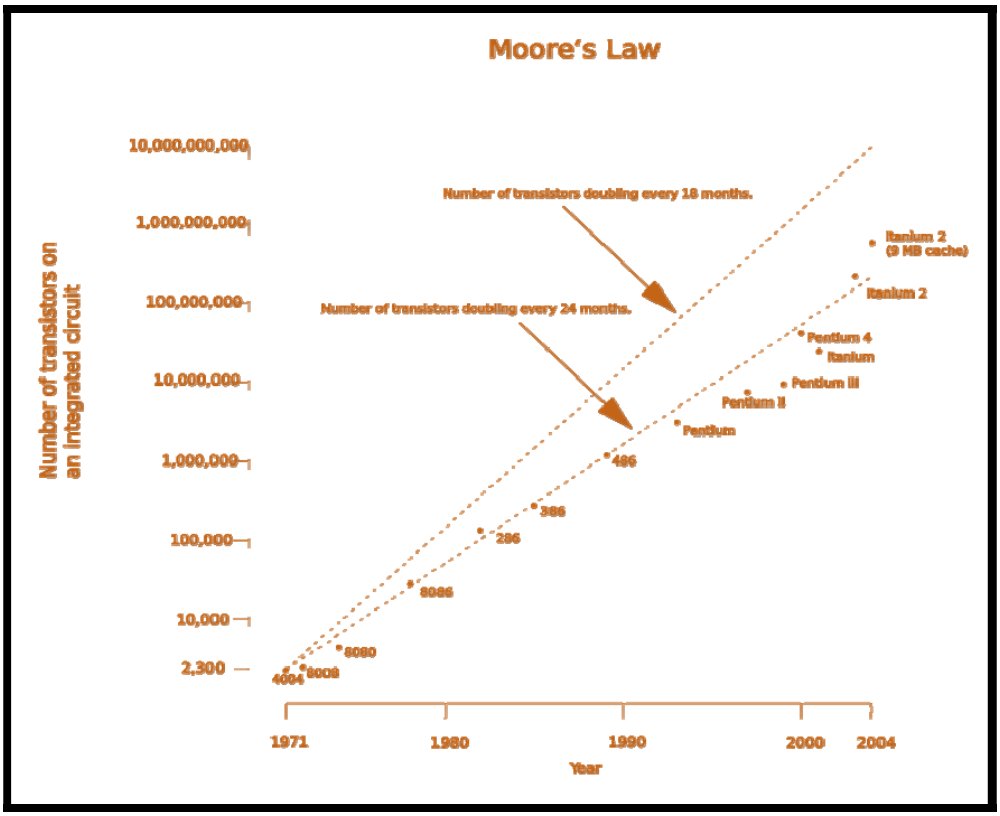
Table 1: Level of circuit integration.

Level	Abbreviation	# Component per Chip
Small Scale Integration	SSI	2 - 50
Medium Scale Integration	MSI	50 - 5000
Large Scale Integration	LSI	5000 – 100, 000
Very Large Scale Integration	VLSI	Over 100, 000

In 1965, George Moore, founder of Intel, made his prediction, popularly known as Moore's Law, which states that the number of transistors on a chip will double about every two years as shown in Figure 2. This prediction has been proven to be accurate that the industry uses it to predict technical advancement. The latest chips have more than 2 billion transistors (Intel, 2010).

The complexity of these circuits makes it impossible to be verified manually, thus computer-aided techniques are ever more critical. Designers use computer programs to automatically place and route circuit layouts allowing gate-level designs to be built and re-used until the top-level block is achieved. Simulators are then used to verify the functionality of circuits before fabrication of the integrated circuit. Once the design has been fully tested and deemed error-free, it is ready for the physical design process. Here two options are available, through an Application Specific Integrated Circuit (ASIC) directly or through an FPGA (Padmanabhan & Sundari, 2004). The FPGA route is attractive for limited volume production or fast development cycle. It can also be used as prototype before the final circuit as ASIC can be elaborate and costly.

FPGA technology falls under the user-programmable semi-custom technique of integrated circuit (IC) designing (Bouldin, 1992). The semi-custom method allows the designer to used pre-defined library cells to be interconnected to specify internal layers. FPGA, in engineering education, is a developed platform that provides an alternative approach to perform almost all the experiments of digital design courses (Mihhailov, et al., 2008). Among the many advantages this practice offers is that it is cost-effective, hassle free and time efficient in performing laboratory experiments (Ali, et al., 2007).



Source: Intel, 2010

Figure 2: Moore's law.

Countries like Taiwan have long seen the benefits of using FPGA. It has established the Chip Implementation Centre (CIC) for promoting FPGA based education and research (Chang, 2002), joining universities like Purdue University (O'keefe, et al., 1989), South Dakota State University (Andrawis, 1997) which as early as the 1990's, have been introducing VLSI and FPGA courses in their curriculum. In courses related to computer architecture, the methodology of different types of processor design and implementation using FPGA are being taught (Hamblem, et al., 1999).

Figure 3 illustrates the FPGA design flow (Altera, 2009) normally followed in FPGA prototyping courses. The Computer Aided Design (CAD) flow starts with the specification of the desired circuit design. It can be entered by means of a schematic diagram, or by using a hardware description language, such as Verilog or Very High-speed Integrated Circuit Hardware Description Language (VHDL). This is followed by the synthesis where the design is synthesized into a circuit that consists of the logic elements (LEs) provided in the FPGA chip. Simulation can be done to verify functional correctness. After verifying correctness, the circuit is fitted into the actual FPGA chip where it is routed for the required connections. Then come analysis and simulation of timing characteristics to verify performance expectations. Once verified, the designed circuit is implemented in a physical FPGA chip by programming the board.

Along the implementation of the process flow lie some shortcomings. While most undergraduate courses teach Hardware Description Languages (HDLs) and FPGA design as part of their digital design courses, they lack what the industry requires for the following reason: most digital design course simply tackle FPGA prototyping by describing it in HDL syntaxes which is normally covered by digital design textbooks (Wakerly, 2005 and Cilletti, 2002). To bring this up to industry-grade level, graduates must be able to completely write codes that are efficiently implemented in an FPGA or any target device. In other words, they need to learn how to synthesize and optimize the codes.

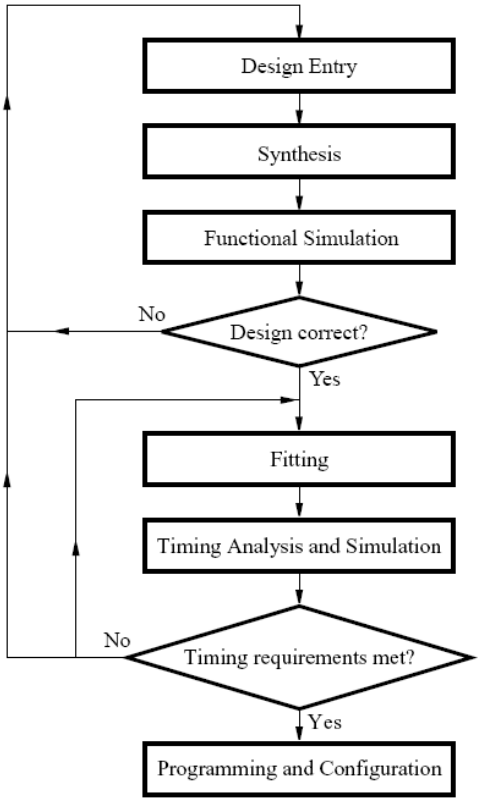


Figure 3: FPGA design flow.

According to Greenwood (2009), the main reason for this problem is time. With the time spent on teaching the basics of digital design, from flip-flops to state machines, not much is left to cover the critical parts of FPGA prototyping: HDL syntaxes and design hierarchies, test-bench writing, synthesizing and optimizing codes. To Greenwood, "Digital design and digital synthesis are best learned in completely separate courses where the two topics won't interfere with each other and each can be presented in sufficient depth".

MALAYSIA INITIATIVE

The Malaysian government understands the gap between what this niche industry requires and academe teaches. This need for more knowledgeable engineers is also necessitated by the fact that Malaysia has substantial numbers of multinational companies (MNCs) in manufacturing and electronics. Most are situated in the states of Penang and Kedah, Johor and Selangor.

Various agencies have been mobilized to narrow down this gap. One key agency is the Multimedia Development Corporation or MDeC which directs and oversees Malaysia's National ICT (Information & Communication Technology) Initiative (MDeC, n.d.). MDeC is committed to make Malaysia a preferred location for ICT and multimedia innovations, operations and services. Its mandate to promote and develop ICT in Malaysia has provided to be a strong impetus for the academe and industry collaboration.

Under its Industry Academia Collaboration scheme (MSC, n.d.), IHLs, more notably universities, will serve as "anchor suppliers" of fresh graduates to Multinational Companies (MNCs). One of the activities to achieve this aim is though the Train-the-Trainer program. Part of the program is to get the MNC to give technical support and facilitate technology transfer. Altera, a semiconductor giant, as one of the companies that is part of this program, spent US$100,000 (RM330,000) to inject its industrial expertise into the current engineering curricula used at local universities and colleges. The investment includes the donation of 600 design boards, the company's Quartus II semiconductor design software and textbooks to set-up a VLSI design laboratory in 10 local universities (Thestaronline, 2008).

The VLSI Train-the-Trainer program was the result of this collaboration. A group of lecturers from all over the country were invited to attend this week-long intensive seminar-workshop covering the structure of FPGA prototyping and Verilog HDL education. MDEC provided much of the funding, hiring industry competent third-party trainers while Altera supplied the DE1 and DE2 hardware as well as laboratory materials with test oscilloscopes on loan from Agilent Technologies. Multiple Verilog-HDL prototyping experiments, using the Quartus II software, were included in the course ranging from the basic to more advance topics. In addition, representatives from Altera introduced the latest available FPGA tools, techniques and practices.

DEVELOPING AN INTERNAL TRAINING PROGRAM

Rising to meet the above-mentioned challenges and armed with the knowledge gained from the MDEC-Altera VLSI Train-the-Trainer program, the Engineering Department of KDU College Penang came up with the internal three-month training program. With 4 lecturers equipped with industry-based skills, the training program was conceptualized in April, 2009. The hardware, the DE1 board, and software (Quartus II) were provided by Altera. By May, the first batch of 9 students from the B.Eng (Hons) in Electrical and Electronics Engineering awarded by Northumbria University, UK program had enrolled. Another set of 3 students from the same degree joined the program in October, 2009 as the second batch.

The main aim of the program is to provide an active learning center for FPGA education. Central to this objective is teaching the students to take the learning initiative. To develop this independent-learning mindset, the students were tasked to develop a working arcade-type game console prototype, with a title of their own choosing, within the three-month period. Materials for learning, the DE1 boards and Quartus II software were provided to the participants. Trainees, at the end of their training period, must conduct a product presentation and produce reflective reports depicting the methods used, analysis and conclusions.

The training employs a holistic approach to the student's development. Apart from the technical objectives, it aims to develop skills in group-team dynamics, promoting cooperation and communication. By taking the trainees on as full-time staff for the whole training period, the sense of organisational culture instills corporate responsibilities and policies. They are given their own working cubicles outfitted with PCs, printers and internet connection, as well as the required clocking in and out combined with other Human Resource and Administrative functions applicable to complete the simulated corporate environment.

Though the training provides an independent learning approach, the trainees were still provided with technical supervision by the lecturers. Initial hesitation had been noted among the trainees. While this is normal, the students-trainees were reassured that with proper training materials and time allocation, the result will be forthcoming provided their initiatives to learn were present. Continuous consultations throughout the training period were done to monitor and guide the trainees. This motivation and mentoring is another component of the holistic approach which is generally not present in the classroom-based learning environment normally conducted.

The three-month training program is divided into 3-phases. The first phase involves introducing the trainees to the basics of the Verilog-HDL and Altera DE1 board. Here the history and development of programmable logic devices, architecture, tools and design flows are covered. All trainees are given a compilation of training materials on CD. The team of lecturers deemed this collection of materials sufficient enough as a start-up kit which consisted of licensed tutorial materials from the MDeC training and online laboratory resources from the Altera website as well as a list of online links and websites relevant to the training. Simulation and synthesis are done using the web edition of Quartus II, version 8.0, on the DE1 board. At this stage, trainees are taught about hierarchies, instantiation, port manipulation and connections. The first phase takes two to three weeks to complete.

The second phase focuses on the DE1 board's component functionalities and communication with external devices attached using extension headers as provided in the board. This includes VGA interfacing, LCD displays, memory modules, and human interface devices (HID) like the keyboard and mouse which provide external controls for the development of a game console which is so far the students' most common outcome of this training.

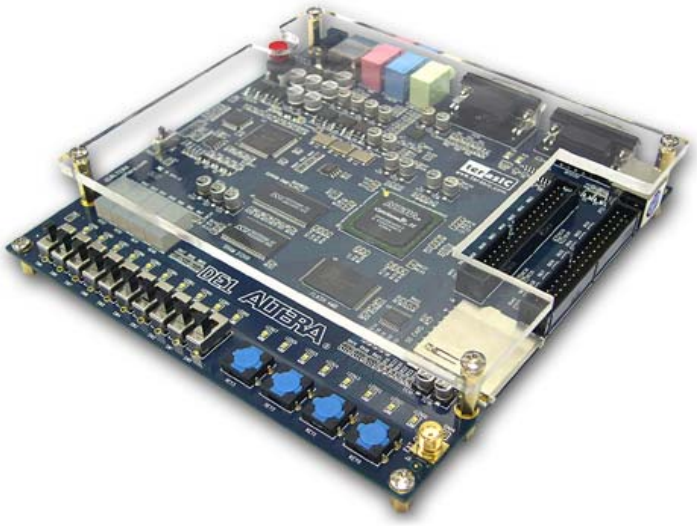
The third and final phase of the program is fully focused on the final product. At this stage, the trainees are given much more time to concentrate on their chosen projects. The emphasis now is on writing synthesizable Register-Transfer-Logic (RTL) codes. Here, the students are allowed to take full credit for their design. No implementation guidelines are given. As the tasks at this stage are more complex than the laboratory exercises, trainees work in groups. Towards the later part of this stage, the trainees are advised to complete their report with emphasis on results and analysis from what the Quartus II generates.

Presentation and demonstration of the working product are the last assignments each trainee performs. This stage is performs to assess the oral communication skills as well as confidence and credibility of the trainees. A formal presentation setup enabled the trainees to get the feel of how it is to "sell" their products to an audience. Those in the audience for the first two batches consisted of lower level undergraduate students and lecturers. Questions were raised by the audience and answered appropriately as the students took pride and ownership in their final products.

PRACTICAL EXERCISES

The use of FPGA-based development boards was made possible through the donations of 10 DE1 boards from Altera. For this training program to be successful, intensive practical laboratory exercises are a must as it is crucial in learning Verilog. Each of the trainees was provided with DE1 board (Figure 4). Its reusability and its reprogrammability provide flexibility and explorability.

By the second week, after learning the operational aspect of Quartus II, trainees are already simulating and programming the target board. Most of the laboratory exercises were taken from the Altera website (Altera, n.d.) with modifications to specific areas to provide familiarity and ease of learning. At the moment, most FPGA vendors have programs to support universities on their websites. Their support websites includes examples and tutorials.



Source: Terasic, 2010

Figure 4: Altera DE1 board.

Simulation is an integral part of FPGA prototyping. But it serves more than just to verify design functionality as it plays a big role in learning Verilog syntaxes. Since any error can be remedied easily at no cost, simulation provides a lot of leeway in approaching syntax applications. Students have the opportunity to try something out, see the results and "play" around with the design. As it is an independent learning-based approach, students are free to explore answers to the requirement of each exercise. This hands-on, trial-and-error method allows them to find the most suitable way of tackling problems given in each exercise on their own, proving that "simulation reinforces learning" (Bouldin, 2004).

CONCLUSION AND FUTURE OUTLOOK

The program is barely a one year and half old but very encouraging results have already been noted. In a period of three months, the trainees were able to design, develop and present a working arcade-type game console complete with sounds, graphics and animation.

The second evident result is the increased level of interest to use FPGA concepts in general and more specifically the use of DE1 boards for final year projects. It has raised the level of awareness and quality of undergraduate final year projects. Projects include topics in data encryption, FPGA-based education tools and digital signal processing. Another more subtle outcome was the development of the trainees' soft-skills in terms of organizational communication and teamwork.

Among the positive attributes they got out of the training is that their level of confidence has increased tremendously. Seeing the final product working and being appreciated by others has given them additional impetus in their studies even in other courses. All the apprehension at the beginning of the training period was transformed to motivation to do much more with the newly acquired knowledge in FPGA prototyping. In this aspect, the program was a resounding success.

The arcade-type games developed by the trainees are just the start of what the training can produce. Future plans include carrying out System-on-Chip Programming (SOPC) using Intellectual Property (IP) cores. To do this, additional tools from Altera such as Nios II Development Environment (IDE) as well as higher density Nios and DE boards are needed. This will open up the potential for projects in embedded applications, robotics and imaging technology.

The successful introduction of the training program was the result of the collaboration among industry, government and academic institutions. This partnership was possible due to significant amount of resources, time and money being invested. The other important factor to make this relationship work is that IHLs need to remain open-minded that the efforts by the industry and the government are not meant to undermine their current courses but instead to reinforce these courses and make them more relevant.

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